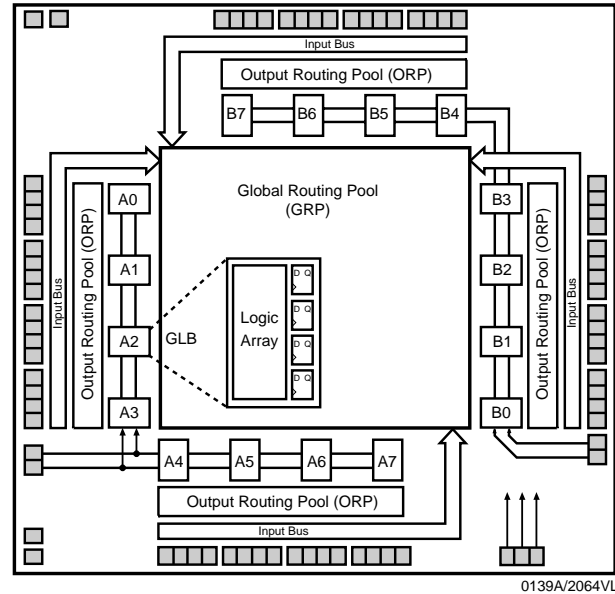


## Features

- **SuperFAST HIGH DENSITY PROGRAMMABLE LOGIC**
  - 2000 PLD Gates
  - 64 and 32 I/O Pin Versions, Four Dedicated Inputs
  - 64 Registers
  - High Speed Global Interconnect
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - 100% Functional, JEDEC and Pinout Compatible with ispLSI 2064V and 2064VE Devices
- **2.5V LOW VOLTAGE 2064 ARCHITECTURE**
  - Interfaces with Standard 3.3V TTL Devices (Inputs and I/Os are 3.3V Tolerant)
  - 60 mA Typical Active Current
- **HIGH-PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY**
  - $f_{max} = 165\text{MHz}$  Maximum Operating Frequency
  - $t_{pd} = 5.5\text{ns}$  Propagation Delay
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - 100% Tested at Time of Manufacture
  - Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - 2.5V In-System Programmability (ISP<sup>™</sup>) Using Boundary Scan Test Access Port (TAP)
  - Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR or Bus Arbitration Logic
  - Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - Reprogram Soldered Devices for Faster Prototyping
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAs**
  - Enhanced Pin Locking Capability
  - Three Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Programmable Output Slew Rate Control
  - Flexible Pin Placement
  - Optimized Global Routing Pool Provides Global Interconnectivity
- **ispDesignEXPERT<sup>™</sup> – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - Superior Quality of Results
  - Tightly Integrated with Leading CAE Vendor Tools
  - Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER<sup>™</sup>
  - PC and UNIX Platforms

## Functional Block Diagram



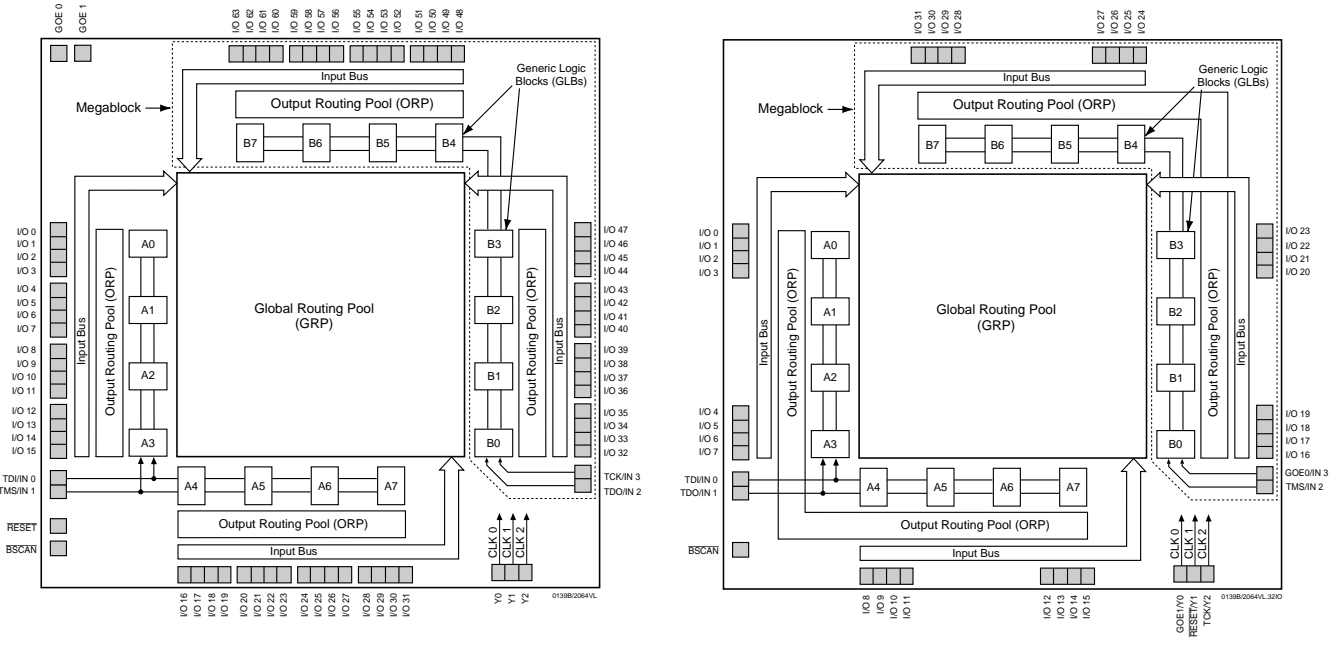
## Description

The ispLSI 2064VL is a High Density Programmable Logic Device available in 64 and 32 I/O-pin versions. The device contains 64 Registers, four Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2064VL features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2064VL offers non-volatile reprogrammability of the logic, as well as the interconnect, to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2064VL device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1...B7 (see Figure 1). There are a total of 16 GLBs in the ispLSI 2064VL device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

**Functional Block Diagram**

**Figure 1. ispLSI 2064VL Functional Block Diagram (64-I/O and 32-I/O Versions)**



The 64-I/O 2064VL contains 64 I/O cells, while the 32-I/O version contains 32 I/O cells. Each I/O cell is directly connected to an I/O pin and can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 3.3V signal levels to support mixed-voltage systems.

Eight GLBs, 32 or 16 I/O cells, two dedicated inputs and two or one ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 or 16 universal I/O cells by two or one ORPs. Each ispLSI 2064VL device contains two Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2064VL device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a

GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

**Programmable Open-Drain Outputs**

In addition to the standard output configuration, the outputs of the ispLSI 2064VL are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration is totem-pole configuration. The open-drain/totem-pole option is selectable through the ispDesignEXPERT software tools.

## Absolute Maximum Ratings <sup>1</sup>

Supply Voltage $V_{CC}$ .....	-0.5 to +4.05V
Input Voltage Applied.....	-0.5 to +4.05V
Off-State Output Voltage Applied .....	-0.5 to +4.05V
Storage Temperature .....	-65 to 150°C
Case Temp. with Power Applied .....	-55 to 125°C
Max. Junction Temp. ( $T_J$ ) with Power Applied .....	150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
$V_{CC}$	Supply Voltage	Commercial $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	2.3	2.7	V
		Industrial $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.3	2.7	V
$V_{IL}$	Input Low Voltage	-0.3	0.7	V	
$V_{IH}$	Input High Voltage	1.7	3.6	V	

Table 2-0005/2064VL

## Capacitance ( $T_A=25^\circ\text{C}$ , $f=1.0\text{ MHz}$ )

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
$C_1$	Dedicated Input Capacitance	8	pf	$V_{CC} = 2.5\text{V}$ , $V_{IN} = 0.0\text{V}$
$C_2$	I/O Capacitance	6	pf	$V_{CC} = 2.5\text{V}$ , $V_{IO} = 0.0\text{V}$
$C_3$	Clock and Global Output Enable Capacitance	10	pf	$V_{CC} = 2.5\text{V}$ , $V_Y = 0.0\text{V}$

Table 2-0006/2064VL

## Erase Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	—	Cycles

Table 2-0008/2064VL

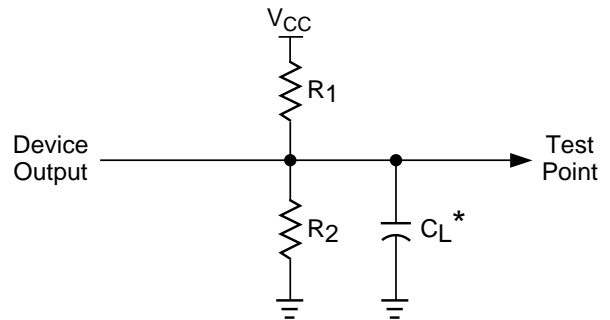
**Switching Test Conditions**

Input Pulse Levels	GND to V <sub>CC</sub>
Input Rise and Fall Time	≤ 1.5 ns 10% to 90%
Input Timing Reference Levels	V <sub>CC</sub> /2
Output Timing Reference Levels	V <sub>CC</sub> /2
Output Load	See Figure 2

3-state levels are measured 0.15V from steady-state active level.

Table 2-0003/2064VL

**Figure 2. Test Load**



\*C<sub>L</sub> includes Test Fixture and Probe Capacitance.

0213A/2064VL

**Output Load Conditions (see Figure 2)**

TEST CONDITION		R1	R2	CL
A		250Ω	218Ω	35pF
B	Active High	∞	218Ω	35pF
	Active Low	250Ω	∞	35pF
C	Active High to Z at V <sub>OH</sub> -0.15V	∞	218Ω	5pF
	Active Low to Z at V <sub>OL</sub> +0.15V	250Ω	∞	5pF

Table 2-0004/2064VL

**DC Electrical Characteristics**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>3</sup>	MAX.	UNITS
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 100μA	—	—	0.2	V
		I <sub>OL</sub> = 8mA	—	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2	—	—	V
		I <sub>OH</sub> = -1mA	2.0	—	—	V
		I <sub>OH</sub> = -4mA	1.8	—	—	V
I <sub>IL</sub> <sup>5</sup>	Input or I/O Low Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> (Max.)	—	—	-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current	V <sub>IH</sub> (min) ≤ V <sub>IN</sub> ≤ 3.6V	—	—	10	μA
I <sub>IL-isp</sub>	BSCAN Input Pull-Up Current	0V ≤ V <sub>IN</sub> ≤ V <sub>IL</sub>	—	—	-150	μA
I <sub>IL-PU</sub>	I/O Active Pull-Up Current	0V ≤ V <sub>IN</sub> ≤ V <sub>IL</sub>	—	—	-150	μA
I <sub>OS</sub> <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 2.5V, V <sub>OUT</sub> = 0.5V	—	—	-100	mA
I <sub>CC</sub> <sup>2,4</sup>	Operating Power Supply Current	V <sub>IL</sub> = 0.0V, V <sub>IH</sub> = 2.5V f <sub>CLK</sub> = 1 MHz	—	60	—	mA

Table 2-0007/2064VL

- One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
- Measured using four 16-bit counters.
- Typical values are at V<sub>CC</sub> = 2.5V and T<sub>A</sub> = 25°C.
- Maximum I<sub>CC</sub> varies widely with specific device configuration and operating frequency. Refer to Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I<sub>CC</sub>.
- With no pull-up resistors.

## External Timing Parameters

### Over Recommended Operating Conditions

PARAMETER	TEST COND. <sup>3</sup>	#	DESCRIPTION <sup>1</sup>	-165		-135		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>pd1</sub>	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	5.5	—	7.5	—	10.0	ns
t <sub>pd2</sub>	A	2	Data Propagation Delay	—	8.0	—	10.0	—	13.0	ns
f <sub>max</sub>	A	3	Clock Frequency with Internal Feedback <sup>2</sup>	165	—	135	—	100	—	MHz
f <sub>max</sub> (Ext.)	—	4	Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ )	118	—	95	—	77	—	MHz
f <sub>max</sub> (Tog.)	—	5	Clock Frequency, Max. Toggle	166	—	143	—	100	—	MHz
t <sub>su1</sub>	—	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	3.5	—	5.0	—	6.5	—	ns
t <sub>co1</sub>	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	—	4.0	—	4.5	—	5.0	ns
t <sub>h1</sub>	—	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	—	0.0	—	0.0	—	ns
t <sub>su2</sub>	—	9	GLB Reg. Setup Time before Clock	4.5	—	6.0	—	8.0	—	ns
t <sub>co2</sub>	A	10	GLB Reg. Clock to Output Delay	—	5.0	—	5.5	—	6.0	ns
t <sub>h2</sub>	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	0.0	—	ns
t <sub>r1</sub>	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	—	6.0	—	8.0	—	13.5	ns
t <sub>rw1</sub>	—	13	Ext. Reset Pulse Duration	5.0	—	5.5	—	6.5	—	ns
t <sub>ptoen</sub>	B	14	Input to Output Enable	—	10.0	—	12.0	—	15.0	ns
t <sub>ptoedis</sub>	C	15	Input to Output Disable	—	10.0	—	12.0	—	15.0	ns
t <sub>goeen</sub>	B	16	Global OE Output Enable	—	6.0	—	7.0	—	9.0	ns
t <sub>goedis</sub>	C	17	Global OE Output Disable	—	6.0	—	7.0	—	9.0	ns
t <sub>wh</sub>	—	18	External Synchronous Clock Pulse Duration, High	3.0	—	3.5	—	5.0	—	ns
t <sub>wl</sub>	—	19	External Synchronous Clock Pulse Duration, Low	3.0	—	3.5	—	5.0	—	ns

Table 2-0030/2064VL

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

## Internal Timing Parameters<sup>1</sup>

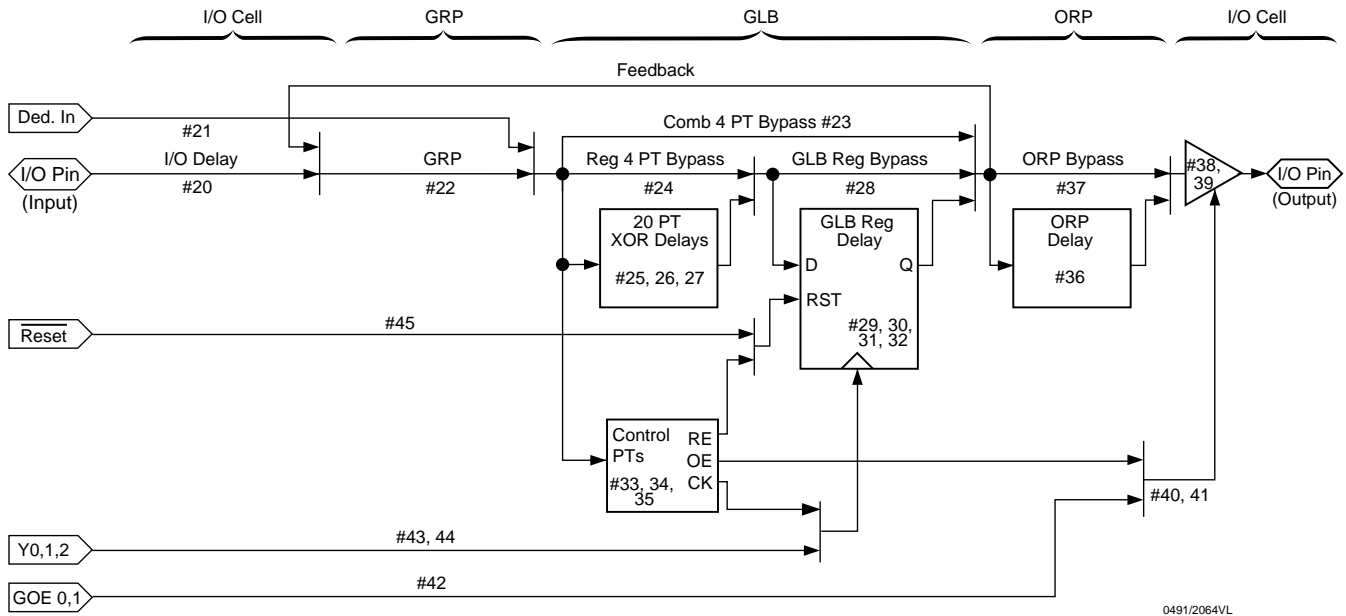
### Over Recommended Operating Conditions

PARAMETER	# <sup>2</sup>	DESCRIPTION	-165		-135		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
<b>Inputs</b>									
<b>t<sub>io</sub></b>	20	Input Buffer Delay	—	0.5	—	1.0	—	0.9	ns
<b>t<sub>din</sub></b>	21	Dedicated Input Delay	—	1.6	—	2.2	—	2.7	ns
<b>GRP</b>									
<b>t<sub>grp</sub></b>	22	GRP Delay	—	1.1	—	1.2	—	1.8	ns
<b>GLB</b>									
<b>t<sub>4ptbpc</sub></b>	23	4 Product Term Bypass Path Delay (Combinatorial)	—	1.9	—	3.2	—	5.2	ns
<b>t<sub>4ptbpr</sub></b>	24	4 Product Term Bypass Path Delay (Registered)	—	2.4	—	3.2	—	4.7	ns
<b>t<sub>1ptxor</sub></b>	25	1 Product Term/XOR Path Delay	—	3.4	—	4.2	—	6.2	ns
<b>t<sub>20ptxor</sub></b>	26	20 Product Term/XOR Path Delay	—	3.4	—	4.2	—	6.2	ns
<b>t<sub>xoradj</sub></b>	27	XOR Adjacent Path Delay <sup>3</sup>	—	3.4	—	4.2	—	6.2	ns
<b>t<sub>gbp</sub></b>	28	GLB Register Bypass Delay	—	0.0	—	0.5	—	1.0	ns
<b>t<sub>gsu</sub></b>	29	GLB Register Setup Time before Clock	1.2	—	1.7	—	1.7	—	ns
<b>t<sub>gh</sub></b>	30	GLB Register Hold Time after Clock	2.3	—	3.3	—	4.8	—	ns
<b>t<sub>gco</sub></b>	31	GLB Register Clock to Output Delay	—	0.3	—	0.3	—	0.3	ns
<b>t<sub>gro</sub></b>	32	GLB Register Reset to Output Delay	—	0.6	—	1.1	—	4.3	ns
<b>t<sub>ptre</sub></b>	33	GLB Product Term Reset to Register Delay	—	4.8	—	6.6	—	8.9	ns
<b>t<sub>ptoe</sub></b>	34	GLB Product Term Output Enable to I/O Cell Delay	—	4.9	—	5.8	—	7.4	ns
<b>t<sub>ptck</sub></b>	35	GLB Product Term Clock Delay	1.1	4.1	2.1	4.5	2.8	4.8	ns
<b>ORP</b>									
<b>t<sub>orp</sub></b>	36	ORP Delay	—	1.4	—	1.5	—	1.5	ns
<b>t<sub>orpbp</sub></b>	37	ORP Bypass Delay	—	0.4	—	0.5	—	0.5	ns
<b>Outputs</b>									
<b>t<sub>ob</sub></b>	38	Output Buffer Delay	—	1.6	—	1.6	—	1.6	ns
<b>t<sub>sl</sub></b>	39	Output Slew Limited Delay Adder	—	2.0	—	2.0	—	2.0	ns
<b>t<sub>oen</sub></b>	40	I/O Cell OE to Output Enabled	—	3.5	—	4.0	—	4.9	ns
<b>t<sub>odis</sub></b>	41	I/O Cell OE to Output Disabled	—	3.5	—	4.0	—	4.9	ns
<b>t<sub>goe</sub></b>	42	Global Output Enable	—	2.5	—	3.0	—	4.1	ns
<b>Clocks</b>									
<b>t<sub>gy0</sub></b>	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.7	1.7	2.1	2.1	2.6	2.6	ns
<b>t<sub>gy1/2</sub></b>	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.9	1.9	2.3	2.3	2.8	2.8	ns
<b>Global Reset</b>									
<b>t<sub>gr</sub></b>	45	Global Reset to GLB	—	3.4	—	4.8	—	7.1	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036/2064VL

**ispLSI 2064VL Timing Model**



0491/2064VL

**Derivations of  $t_{su}$ ,  $t_h$  and  $t_{co}$  from the Product Term Clock**

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{io} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{io} + t_{grp} + t_{ptck(min)}) \\
 &= (\#20 + \#22 + \#26) + (\#29) - (\#20 + \#22 + \#35) \\
 3.5\text{ns} &= (0.5 + 1.1 + 3.4) + (1.2) - (0.5 + 1.1 + 1.1) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{io} + t_{grp} + t_{20ptxor}) \\
 &= (\#20 + \#22 + \#35) + (\#30) - (\#20 + \#22 + \#26) \\
 3.0\text{ns} &= (0.5 + 1.1 + 4.1) + (2.3) - (0.5 + 1.1 + 3.4) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#22 + \#35) + (\#31) + (\#36 + \#38) \\
 9.0\text{ns} &= (0.5 + 1.1 + 4.1) + (0.3) + (1.4 + 1.6)
 \end{aligned}$$

Note: Calculations are based on timing specifications for the ispLSI 2064VL-165L.

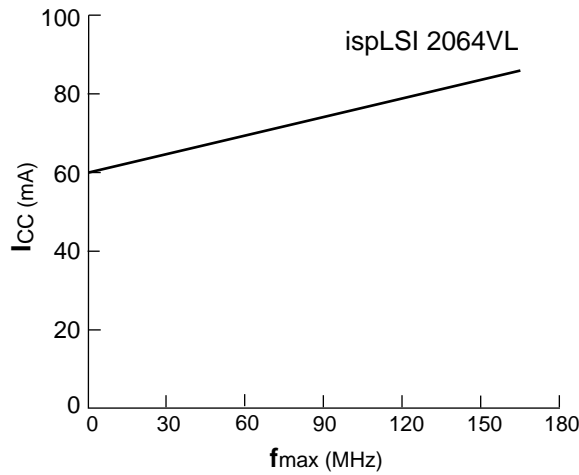
Table 2-0042/2064VL

**Power Consumption**

Power consumption in the ispLSI 2064VL device depends on two primary factors: the speed at which the device is operating and the number of Product Terms

used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**



Notes: Configuration of four 16-bit counters  
Typical current at 2.5V, 25° C

ICC can be estimated for the ispLSI 2064VL using the following equation:

$$I_{CC}(mA) = 8 + (\# \text{ of PTs} * 0.42) + (\# \text{ of Nets} * \text{Max. Freq.} * 0.0025)$$

Where:

- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The ICC estimate is based on typical conditions (VCC = 2.5V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

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## 64-I/O Signal Descriptions

Signal Name	Description
RESET	Active Low (0) Reset pin resets all the registers in the device.
GOE 0, GOE1	Global Output Enable input pins.
Y0, Y1, Y2	Dedicated Clock Input – These clock inputs are connected to one of the clock inputs of all the GLBs in the device.
BSCAN	Input – Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	Input – This pin performs two functions. When BSCAN is logic low, it functions as an input pin to load programming data into the device. When BSCAN is high, it functions as a dedicated input pin.
TCK/IN 3	Input – This pin performs two functions. When BSCAN is logic low, it functions as a clock pin for the Boundary Scan state machine. When BSCAN is high, it functions as a dedicated input pin.
TMS/IN 1	Input – This pin performs two functions. When BSCAN is logic low, it functions as a mode control pin for the Boundary Scan state machine. When BSCAN is high, it functions as a dedicated input pin.
TDO/IN 2	Output/Input – This pin performs two functions. When BSCAN is logic low, it functions as an output pin to read serial shift register data. When BSCAN is high, it functions as a dedicated input pin.
GND	Ground (GND)
VCC	Vcc
NC <sup>1</sup>	No Connect
I/O	Input/Output Pins – These are the general purpose I/O pins used by the logic array.

1. NC pins are not to be connected to any active signals, VCC or GND.

## 32-I/O Signal Descriptions

Signal Name	Description
GOE 0/IN 3	This pin performs one of two functions. It can be programmed to function as a Global Output Enable pin or a Dedicated Input pin.
GOE 1/Y0	This pin performs one of two functions. It can be programmed to function as a Global Output Enable or a Dedicated Clock input. This clock input is connected to one of the clock inputs of all GLBs on the device.
RESET/Y1	This pin performs two functions: (1) Dedicated clock input. This clock input is brought into the Clock Distribution Network and can optionally be routed to any GLB and/or I/O cell on the device. (2) Active Low (0) Reset pin which resets all of the registers in the device.
BSCAN	Input – Dedicated in-system programming Boundary Scan Enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	Input – This pin performs two functions. When BSCAN is logic low, it functions as an input pin to load programming data into the device. TDI/IN0 is also used as one of the two control pins for the ISP State Machine. When BSCAN is high, it functions as a dedicated input pin.
TMS/IN 2	Input – This pin performs two functions. When BSCAN is logic low, it functions as a pin to control the operation of the ISP State Machine. When BSCAN is high, it functions as a dedicated input pin.
TDO/IN 1	Output/Input – This pin performs two functions. When BSCAN is logic low, it functions as an output pin to read serial shift register data. When BSCAN is high, it functions as a dedicated input pin.
TCK/Y2	Input – This pin performs two functions. When BSCAN is logic low, it functions as a clock pin for the Serial Shift Register. When BSCAN is high, it functions as a dedicated clock input. This clock input is brought into the Clock Distribution Network and can optionally be routed to any GLB and/or I/O cell on the device.
GND	Ground (GND)
VCC	Vcc
NC <sup>1</sup>	No Connect
I/O	Input/Output pins – These are the general purpose I/O pins used by the logic array.

1. NC pins are not to be connected to any active signals, VCC or GND.

## 64-I/O Signal Locations

Signal	100-Ball caBGA	100-Pin TQFP
RESET	D2	11
GOE 0, GOE 1	F9, E1	62, 13
Y0, Y1, Y2	E3, F6, F8	10, 65, 60
BSCAN	E5	15
TDI/IN 0	F2	16
TCK/IN 3	G10	59
TMS/IN 1	J5	37
TDO/IN 2	B6	87
GND	B7, F1, G9, K6	14, 39, 61, 86
VCC	A5, E2, F10, J4	12, 36, 63, 89
NC <sup>1</sup>	A6, A8, C3, C4, D1, D6, D8, E7, E9, E10, F4, G3, G5, H7, H8, K3, K5	4, 9, 21, 25, 31, 38, 44, 50, 54, 64, 66, 71, 75, 81, 88, 94, 100

1. NC pins are not to be connected to any active signals, VCC or GND.

## I/O Locations

Signal	100 caBGA	100 TQFP	44 TQFP	44 PLCC
I/O 0	G1	17	9	15
I/O 1	F3	18	10	16
I/O 2	E4	19	11	17
I/O 3	H1	20	12	18
I/O 4	G2	22	13	19
I/O 5	J1	23	14	20
I/O 6	H2	24	15	21
I/O 7	K1	26	16	22
I/O 8	J2	27	19	25
I/O 9	K2	28	20	26
I/O 10	H3	29	21	27
I/O 11	J3	30	22	28
I/O 12	G4	32	23	29
I/O 13	H4	33	24	30
I/O 14	K4	34	25	31
I/O 15	H5	35	26	32
I/O 16	F5	40	31	37
I/O 17	J6	41	32	38
I/O 18	K7	42	33	39
I/O 19	H6	43	34	40
I/O 20	K8	45	35	41
I/O 21	G6	46	36	42
I/O 22	J7	47	37	43
I/O 23	K9	48	38	44
I/O 24	J8	49	41	3
I/O 25	K10	51	42	4
I/O 26	J9	52	43	5
I/O 27	J10	53	44	6
I/O 28	H9	55	1	7
I/O 29	H10	56	2	8
I/O 30	G7	57	3	9
I/O 31	G8	58	4	10
I/O 32	D10	67	—	—
I/O 33	E8	68	—	—
I/O 34	F7	69	—	—
I/O 35	C10	70	—	—
I/O 36	D9	72	—	—
I/O 37	B10	73	—	—
I/O 38	C9	74	—	—
I/O 39	A10	76	—	—
I/O 40	B9	77	—	—
I/O 41	A9	78	—	—
I/O 42	C8	79	—	—
I/O 43	B8	80	—	—
I/O 44	D7	82	—	—
I/O 45	C7	83	—	—
I/O 46	A7	84	—	—
I/O 47	C6	85	—	—
I/O 48	E6	90	—	—
I/O 49	B5	91	—	—
I/O 50	A4	92	—	—
I/O 51	C5	93	—	—
I/O 52	A3	95	—	—
I/O 53	D5	96	—	—
I/O 54	B4	97	—	—
I/O 55	A2	98	—	—
I/O 56	B3	99	—	—
I/O 57	A1	1	—	—
I/O 58	B2	2	—	—
I/O 59	B1	3	—	—
I/O 60	C2	5	—	—
I/O 61	C1	6	—	—
I/O 62	D4	7	—	—
I/O 63	D3	8	—	—

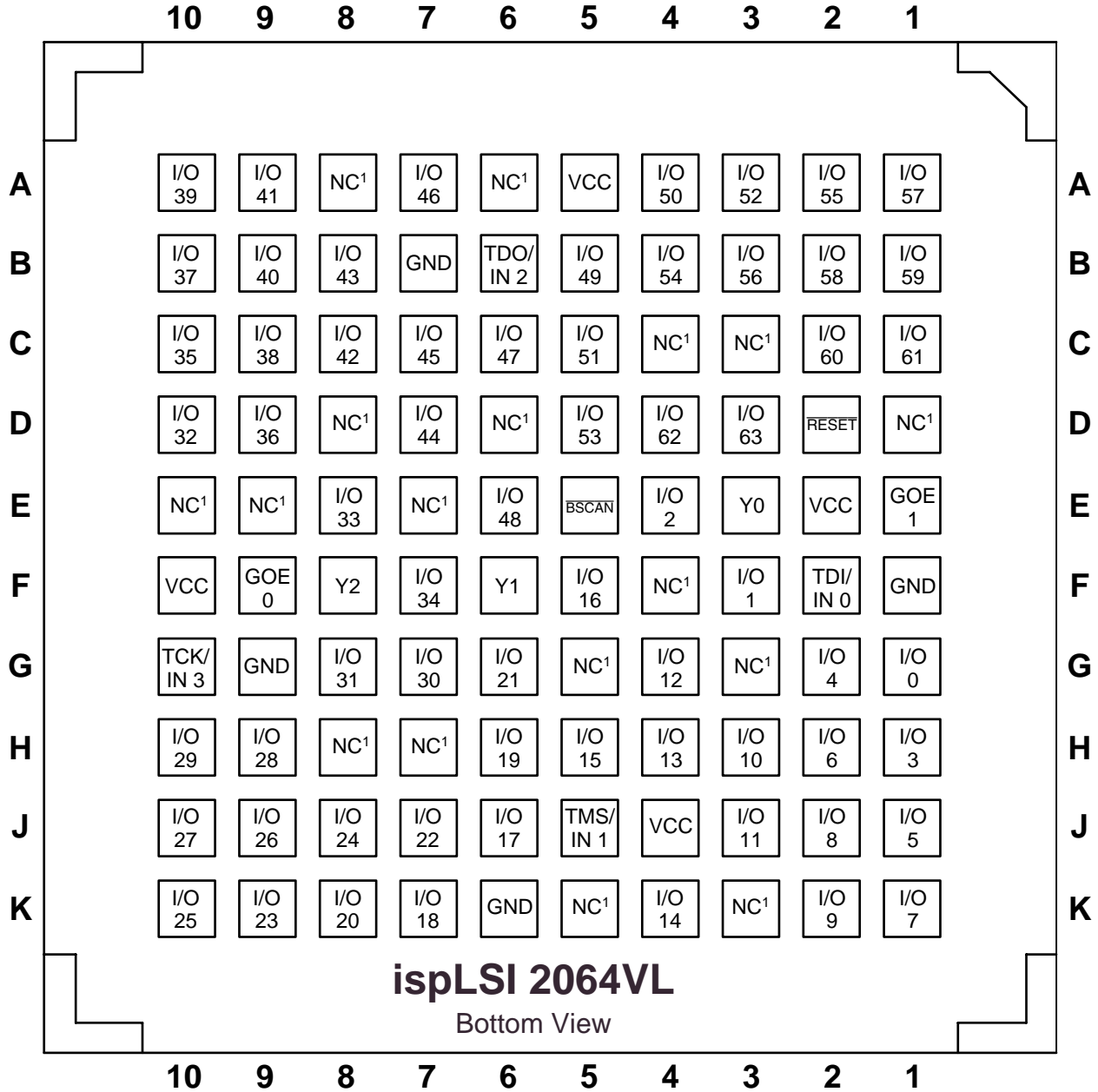
## 32-I/O Signal Locations

Signal	44-Pin TQFP	44-Pin PLCC
GOE 0/ IN 3	40	2
GOE 1/Y0	5	11
RESET/Y1	29	35
BSCAN	7	13
TDI/IN 0	8	14
TMS/IN 2	30	36
TDO/IN 1	18	24
TCK/Y2	27	33
GND	17, 39	1, 23
VCC	6, 28	12, 34
NC <sup>1</sup>	—	—

1. NC pins are not to be connected to any active signals, VCC or GND.

**Signal Configuration**

ispLSI 2064VL 100-Ball caBGA Signal Diagram



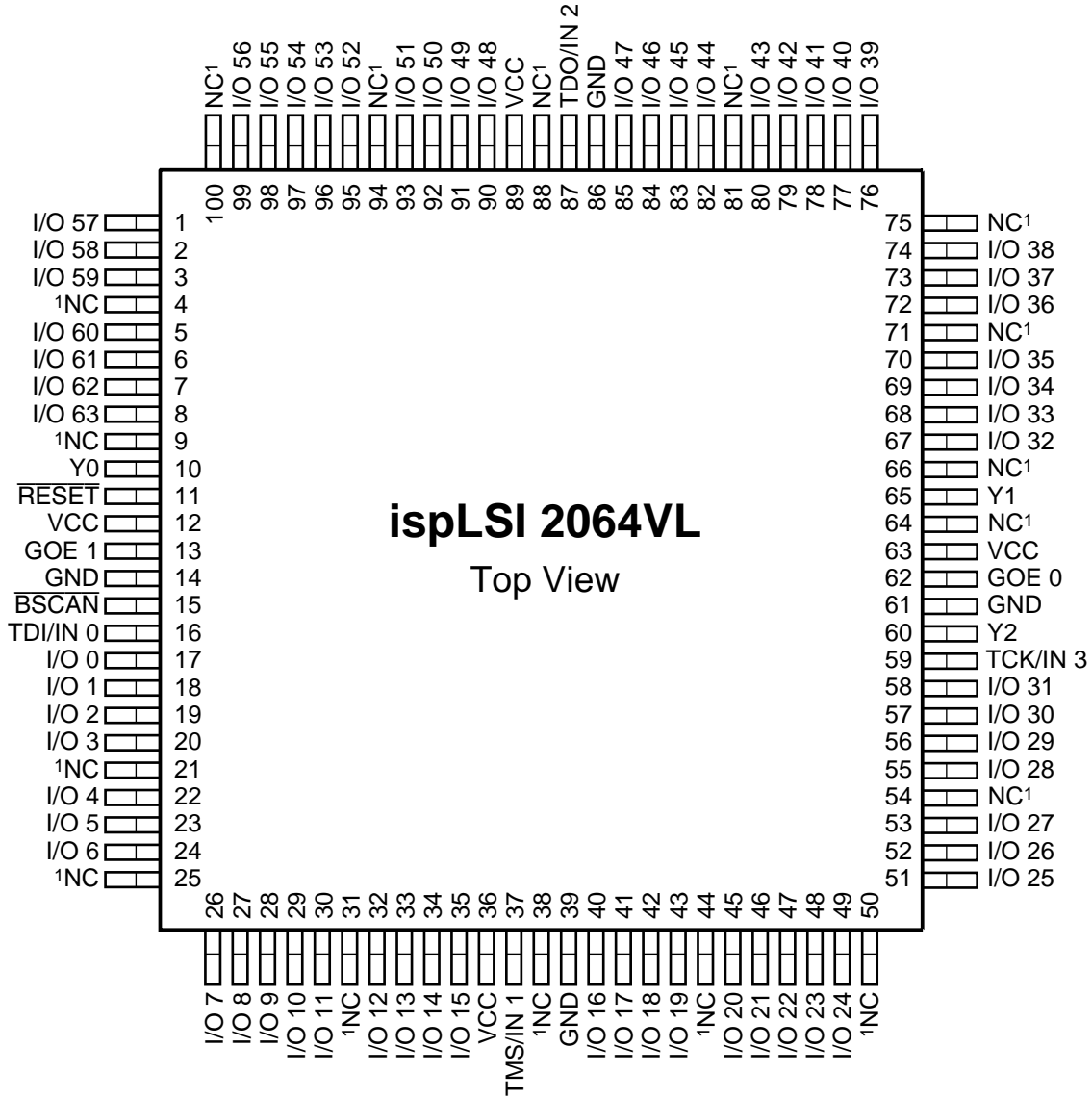
100-BGA/2064VL

<sup>1</sup>NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

**Pin Configuration**

ispLSI 2064VL 100-Pin TQFP Pinout Diagram

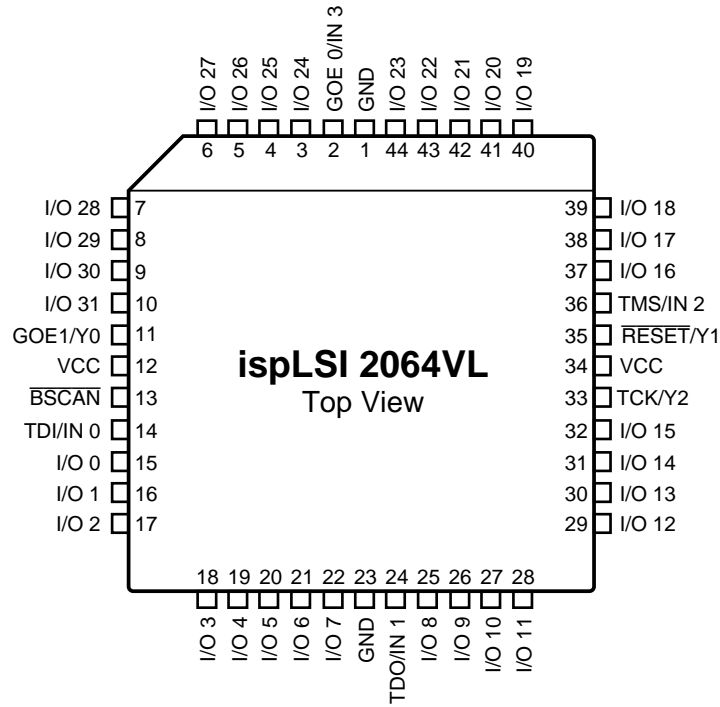


100 TQFP/2064VL

1. NC pins are not to be connected to any active signals, VCC or GND.

**Pin Configuration**

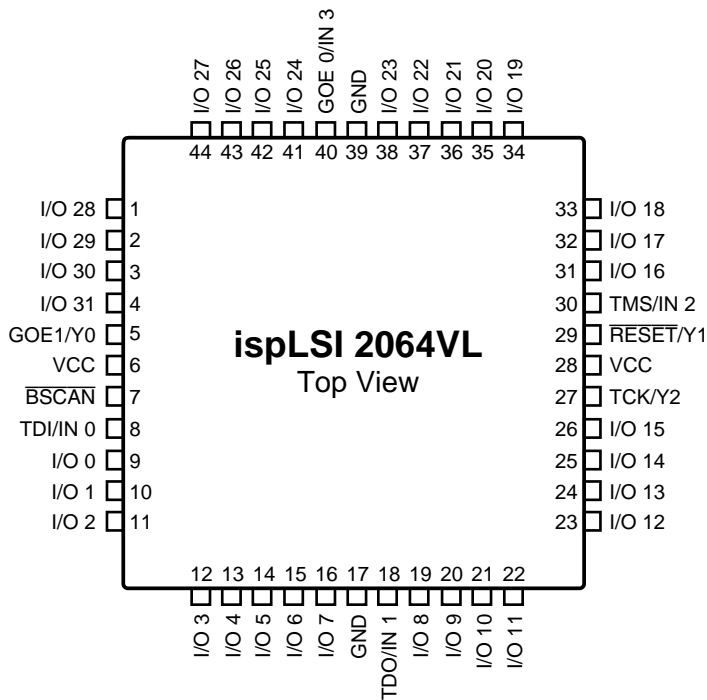
ispLSI 2064VL 44-Pin PLCC Pinout Diagram



44 PLCC/2064VL

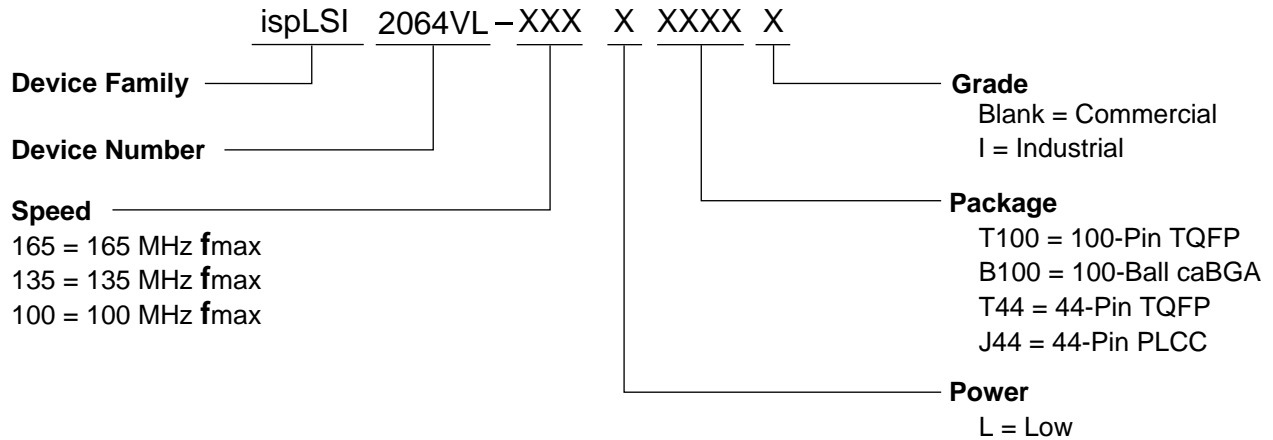
**Pin Configuration**

ispLSI 2064VL 44-Pin TQFP Pinout Diagram



44 TQFP/2064VL

## Part Number Description



0212/2064VL

## ispLSI 2064VL Ordering Information

### COMMERCIAL

FAMILY	<i>f</i> <sub>max</sub> (MHz)	<i>t</i> <sub>pd</sub> (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	165	5.5	64	ispLSI 2064VL-165LT100	100-Pin TQFP
	165	5.5	64	ispLSI 2064VL-165LB100	100-Ball caBGA
	165	5.5	32	ispLSI 2064VL-165LJ44	44-Pin PLCC
	165	5.5	32	ispLSI 2064VL-165LT44	44-Pin TQFP
	135	7.5	64	ispLSI 2064VL-135LT100	100-Pin TQFP
	135	7.5	64	ispLSI 2064VL-135LB100	100-Ball caBGA
	135	7.5	32	ispLSI 2064VL-135LJ44	44-Pin PLCC
	135	7.5	32	ispLSI 2064VL-135LT44	44-Pin TQFP
	100	10	64	ispLSI 2064VL-100LT100	100-Pin TQFP
	100	10	64	ispLSI 2064VL-100LB100	100-Ball caBGA
	100	10	32	ispLSI 2064VL-100LJ44	44-Pin PLCC
	100	10	32	ispLSI 2064VL-100LT44	44-Pin TQFP

Table 2-0041A/2064VL

### INDUSTRIAL

FAMILY	<i>f</i> <sub>max</sub> (MHz)	<i>t</i> <sub>pd</sub> (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	135	7.5	64	ispLSI 2064VL-135LT100I	100-Pin TQFP
	135	7.5	32	ispLSI 2064VL-135LT44I	44-Pin TQFP

Table 2-0041B/2064VL